OrCAD PLD COMPILER V4.02 2/7/91 (Source file .\256KV10.PLD)

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  1  This file contains the logic necessary for a GAL22V10 to perform bank
  2  selection and Write Enable (\WE) for the eight 4464 (64Kx4) dynamic memory
  3  chips on the Micro Innovations 64/256K memory board.  It latches data
  4  lines D0 and D1 and then decodes them into 1 of 4 outputs B0 through B3
  5  to select the appropriate 64K memory bank.  Each of the bank select
  6  lines (B0-B3) also enables the Write Enable (\WE) line for the selected
  7  bank.
  8
  9  |GAL22V10  1:CLK,  4:D0,   5:D1,   8:RW,   14:WE0, 15:WE1,
 10  |          16:B0,  17:B1,  18:B2,  19:B3,  20:WE2, 21:WE3,
 11  |          22:D0L, 23:D1L
 12  |
 13  |          Low: B[0..3], WE[0..3], RW
 14  |
 15  |          D0L = CLK \\ D0
 16  |          D1L = CLK \\ D1
 17  |          B0 = D1L' & D0L'
 18  |          B1 = D1L' & D0L
 19  |          B2 = D1L & D0L'
 20  |          B3 = D1L & D0L
 21  |          WE0 = B0 & RW
 22  |          WE1 = B1 & RW
 23  |          WE2 = B2 & RW
 24  |          WE3 = B3 & RW
 25  |          Signature: "256Krev1"
```

♀RESOLVED EXPRESSIONS (Reduction 2)

Signal name	Row	Terms
D0L	11	D0
D1L	2	D1
B0	99	D0L' D1L'
B1	84	D0L D1L'
B2	67	D0L' D1L
B3	50	D0L D1L
WE0	123	RW B0
WE1	112	RW B1
WE2	35	RW B2
WE3	22	RW B3

♀SIGNAL ASSIGNMENT

Pin	Signal name	Column	Rows Beg	Rows Avail	Rows Used	Activity	
1.	CLK	0	-	-	-	High	(Clock)

2.	-	4	-	-	-		
3.	-	8	-	-	-		
4.	D0	12	-	-	-	High	
5.	D1	16	-	-	-	High	
6.	-	20	-	-	-		
7.	-	24	-	-	-		
8.	RW	29	-	-	-	Low	
9.	-	32	-	-	-		
10.	-	36	-	-	-		
11.	-	40	-	-	-		
13.	-	42	-	-	-		
14.	WE0	39	122	9	1	Low	(Three-state)
15.	WE1	35	111	11	1	Low	(Three-state)
16.	B0	31	98	13	1	Low	(Three-state)
17.	B1	27	83	15	1	Low	(Three-state)
18.	B2	23	66	17	1	Low	(Three-state)
19.	B3	19	49	17	1	Low	(Three-state)
20.	WE2	15	34	15	1	Low	(Three-state)
21.	WE3	11	21	13	1	Low	(Three-state)
22.	D0L	7	10	11	1	High	(Registered)
23.	D1L	3	1	9	1	High	(Registered)
25.	-	-	0	1	0		
26.	-	-	131	1	0		
				----	----		
				132	10	(8%)	

I200 No fatal errors found in source code.
I201 No warnings.

♀OrCAD PLD
Type: PAL22V10
*
QP24* QF5828* QV1024*
F0*
L0044 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0088 11 11 11 11 11 11 11 11 01 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0440 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0484 11 11 11 11 11 11 11 01 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0924 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0968 11 11 11 11 11 11 11 11 11 10 11 11 11 11 10 11 11 11 11 11 11 11 11 11 *
L1496 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1540 11 11 11 11 11 11 11 11 11 11 11 10 11 11 10 11 11 11 11 11 11 11 11 11 *
L2156 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2200 11 10 11 10 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2904 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2948 11 10 11 01 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L3652 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L3696 11 01 11 10 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L4312 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L4356 11 01 11 01 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L4884 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L4928 11 11 11 11 11 11 11 11 11 11 11 11 11 11 10 10 11 11 11 11 11 11 11 11 *
L5368 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L5412 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 10 10 11 11 11 11 11 11 11 *
L5808 10 10 01 01 01 01 01 01 01 01 *
C6CB1*

I202 1/1/92 2:46 pm (Wednesday)
I203 Memory utilization 1976/22426 (9%)
I204 Elapsed time 3 seconds

♀